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being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second operating mode includes a default address size of 32 bits.

REMARKS

Claims 1-22 remain pending. In the present Office Action, claims 1-22 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting over copending application Serial No. 09/483,636 in view of one or more of Hammond et al., U.S. Patent No. 5,774,686 ("Hammond"), Pentium Processor Family Developer's Manual Volume 3: Architecture and Programming Manual ("Intel"), and Alpert et al., U.S. Patent No. 5,617,554 ("Alpert"). Claims 1-22 were further rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Hammond, Intel, and Alpert. The drawings were objected to for not illustrating the features of the method claims 17-22. Applicants respectfully traverse these rejections and objections and request reconsideration.

Claims 1-10

Applicants respectfully submit that each of claims 1-10 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication; a control register configured to store an enable indication, wherein said processor is configured to establish an operating mode responsive to said enable indication, said first operating mode indication, and said second operating mode indication".

The Office Action alleges that the above highlighted features of claim 1 are obvious over Hammond in view of Intel. Applicants respectfully submit that the Office Action does not meet its burden of establishing a *prima facie* case of obviousness. For example, the Office Action combines Hammond and Intel to arrive at a teaching in which a control register includes several flags (an extension flag, an instruction set flag, and a

system flag) and a segment descriptor that includes a D bit/B bit. The Office Action then modifies the combination by moving one of the flags from the control register to the segment descriptor. The Office Action alleges that it would be obvious to move the operating mode indicators from the control register to the segment descriptor because it would allow the operating mode to vary automatically depending on which selector is active and would be an advantage over a global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed (Office Action, page 16, paragraph 45).

Irrespective of whether or not the combination of Hammond and Intel is proper, Applicants respectfully submit that there is no teaching or suggestion in Hammond or Intel to make the proposed modification. The Office Action presents no teachings or suggestions from the references to evidence the Office Action's assertion that it would be obvious to move the operating mode indicators from the control register to the segment descriptor because it would allow the operating mode to vary automatically depending on which selector is active. The Office Action presents no teachings or suggestions from the reference to evidence the Office Action's assertion that it would be an advantage over a global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed. Furthermore, Applicants submit that the there is no evidence that generally available knowledge in the art provides the motivation for modification described above. Thus, it appears that impermissible hindsight from Applicants claimed invention is being used to make the modification.

Applicants further submit that it is unclear that the combination of Hammond and Intel, even if modified as suggested by the Office Action, would achieve the alleged advantage over a global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed. Applicants submit that Intel teaches the use of instructions to change the segment selectors in the segment registers. "Other segments can be used by loading their segment selectors into the segment registers" (Intel, page 3-10, third paragraph, last

sentence). "More segments can be made available by loading their segment selectors into these register during program execution" (Intel, page 11-9, first paragraph, last sentence). "There are forms of the MOV instruction to load the visible part of these segment registers [the segment selector, in Figure 11-6]. The invisible part is loaded by the processor" (Intel, page 11-9, second paragraph, last two sentences). Since instructions are used to change the segment selectors in Intel, it would appear that the alleged advantage over a global flag is not achieved by the proposed modification.

Furthermore, Applicants submit that Intel teaches away from the proposed modification. Only one bit in Intel's segment selector (Figure 11-8) is not already used: bit 21 in the upper word. This bit is reserved and set to zero. Generally, Intel teaches that reserved bits should not be used. For example, Figure 10-4 states that reserved bits should not be defined. Figure 10-1 states that bit positions "shown as 0 or 1 are Intel reserved. Do not use. Always set them to the value previously read." Thus, Intel teaches away from using the unused bit 21 to store one of the flags from Hammond's control register.

For at least all of the above-stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-10, being dependent from claim 1, are similarly patentable over the cited art for at least the above-stated reasons as well. Each of claims 2-10 recite additional combinations of features not taught or suggested in the cited art.

Claims 11-16

Applicants respectfully submit that each of claims 11-16 recites a combination of features not taught or suggested in the cited art. For example, claim 11 recites a combination of features including: "said segment descriptor including an operating mode indication...wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state".

The Office Action alleges that the above highlighted features are taught in

Hammond and Intel. Specifically, the Office Action relies on Intel's D bit/B bit to teach "said segment descriptor including an operating mode indication". However, Intel's D bit/B bit is described as follows: "In a code segment, this bit is called the D bit, and it indicates the default length for operands and effective addresses. If the D bit is set, then 32-bit operands and 32-bit effective addressing modes are assumed. If it is clear, then 16-bit operands and addressing modes are assumed" (Intel, page 11-13, third paragraph). "If B = 1, pushes, pops and calls all use 32-bit ESP register; if B = 0, stack operations use the 16-bit SP register" (Intel, page 11-13, fourth paragraph). Thus, the D bit/B bit controls selection between 32 bit and 16 bit addresses. This does not teach or suggest "said segment descriptor including an operating mode indication...wherein said processor is configured to operate in an operating mode in which virtual addresses are *greater than* 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state".

The Office Action also cites Hammond for teaching virtual addresses greater than 32 bits. However, Hammond selects operating modes in which virtual addresses are greater than 32 bits using flags in a control register (Hammond, col. 6, line 61-col. 7, line 9). Additionally, Hammond teaches "In one embodiment, this second instruction set is a 64-bit instruction set which operates using the same format of address generated by segmentation unit 215 (i.e. linear addresses). Since this 64-bit instruction set uses linear addresses, it can address the entire 64-bit virtual address space and does not require segmentation" (Hammond, col. 5, lines 13-18). Thus, when Hammond is operating in 64-bit mode, it appears that segments are not used. These teachings thus teach away from "said segment descriptor including an operating mode indication...wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state".

For at least all of the above-stated reasons, Applicants respectfully submit that claim 11 is patentable over the cited art. Claims 12-16, being dependent from claim 11, are similarly patentable over the cited art for at least the above-stated reasons as well.

Each of claims 12-16 recite additional combinations of features not taught or suggested in the cited art.

Claims 17-22

Applicants respectfully submit that each of claims 17-22 recites a combination of features not taught or suggested in the cited art. For example, claim 17 recites a combination of features including: "establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor". The Office Action alleges that these features are taught in Hammond at col. 6, line 61-col. 7, line 9 and col. 7, lines 34-39. However, col. 6, line 61-col. 7, line 9 are Hammond's teachings of several flags (an extension flag, an instruction set flag, and a system flag) in his control register. This does not teach or suggest "a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor". At col. 7, lines 34-39, Hammond teaches that when the extension flag in the control register is in the enabled state, the processor may operate in various modes (as indicated by other flags in the control register). Again, these teachings do not teach or suggest "a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor" as recited in claim 17. The Office Action relies on Intel to teach the fetching of operands and generating of addresses responsive to the operating mode, citing the D bit/B bit in Intel's segment selector. However, this single bit also does not teach or suggest "a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor" as recited in claim 17. Furthermore, as highlighted above with regard to claim 1, it would not be obvious to modify the teachings of Hammond and Intel to arrive at the above highlighted features of claim 17.

For at least the above-stated reasons, Applicants submit that claim 17 is patentable over the cited art. Claims 18-22, being dependent from claim 17, are similarly patentable over the cited art for at least the above-stated reasons as well. Each of claims 18-22 recite additional combinations of features not taught or suggested in the cited art.

Double Patenting Rejection

Applicants respectfully disagree with the double patenting rejection, at least with respect to some of the claims. However, Applicants respectfully request that the double patenting rejection be held in abeyance until the claims are otherwise indicated as allowable, at which time Applicants will consider the filing of a terminal disclaimer.

Drawing Objection

The Office Action objected to the drawings under 37 C.F.R. § 1.83(a) for not showing the features of the method claims. Applicants respectfully disagree, and submit that the drawings illustrate the various elements which perform various embodiments of the method, and that such illustration is sufficient to meet the requirements of 37 C.F.R. § 1.83(a).

Nonetheless, Applicants submit herewith a new Fig. 13, and have amended the specification to refer to Fig. 13. Applicants submit that the new figure and corresponding description address the drawing objection. Furthermore, Applicants submit that the new figure and corresponding description are not new matter. The new figure and corresponding description are supported throughout the current specification. Additionally, the new figure and corresponding description are clearly supported by claims 17-22. Since claims 17-22 are part of the original disclosure, these claims are not new matter and adding description to the specification that is supported by these claims is also not new matter. Applicants submit that the new Fig. 13 addresses the rejection.

Additionally included in the Request for Approval of Drawing Changes is Fig. 9. Fig. 9 has been amended to address the objection to Fig. 9 by the Official Draftsman. Additionally, the Official Draftsman objected to Fig. 4 (it appears) for not separately labeling views. Applicants respectfully submit that the two views shown in Fig. 4 are labeled separately (e.g. LME=1 vs. LME=0 and reference numeral 60 vs. reference numeral 62). Applicants respectfully request clarification of the objection to Fig. 4.

Information Disclosure Statements (IDSs)

The Office Action states that it is unclear whether the Applicant would like the co-pending applications cited in the IDSs to be listed (Office Action, item 3). Applicants do not wish the co-pending applications to be listed on the face of any patent issuing from the present application. Applicants wish that the co-pending applications be considered, and that the Examiner confirm such consideration in the next action.

Additionally, Applicants file herewith another IDS. Applicants respectfully request consideration of the references in the IDS and a return of the PTO-1449 form included therewith with the Examiner's initials and signature evidencing such consideration.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Conley, Rose, & Tayon, P.C. Deposit Account No. 501505/5500-54700/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☒ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Marked-up Copy of Amended Claims

☐ Marked-up Copy of Amended Paragraphs

☒ Fee Authorization Form authorizing a deposit account debit in the amount of $180 for fees ($180 IDS fee).

☒ Other: IDS including PTO-1449 form and cited references, Submission of Formal Drawings

Respectfully submitted,

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Date: 11/15/02

Marked-up Copy of Amended Claim:

21. (Amended) The method as recited in claim 18 wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said [first] second operating mode includes a default address size of 32 bits.

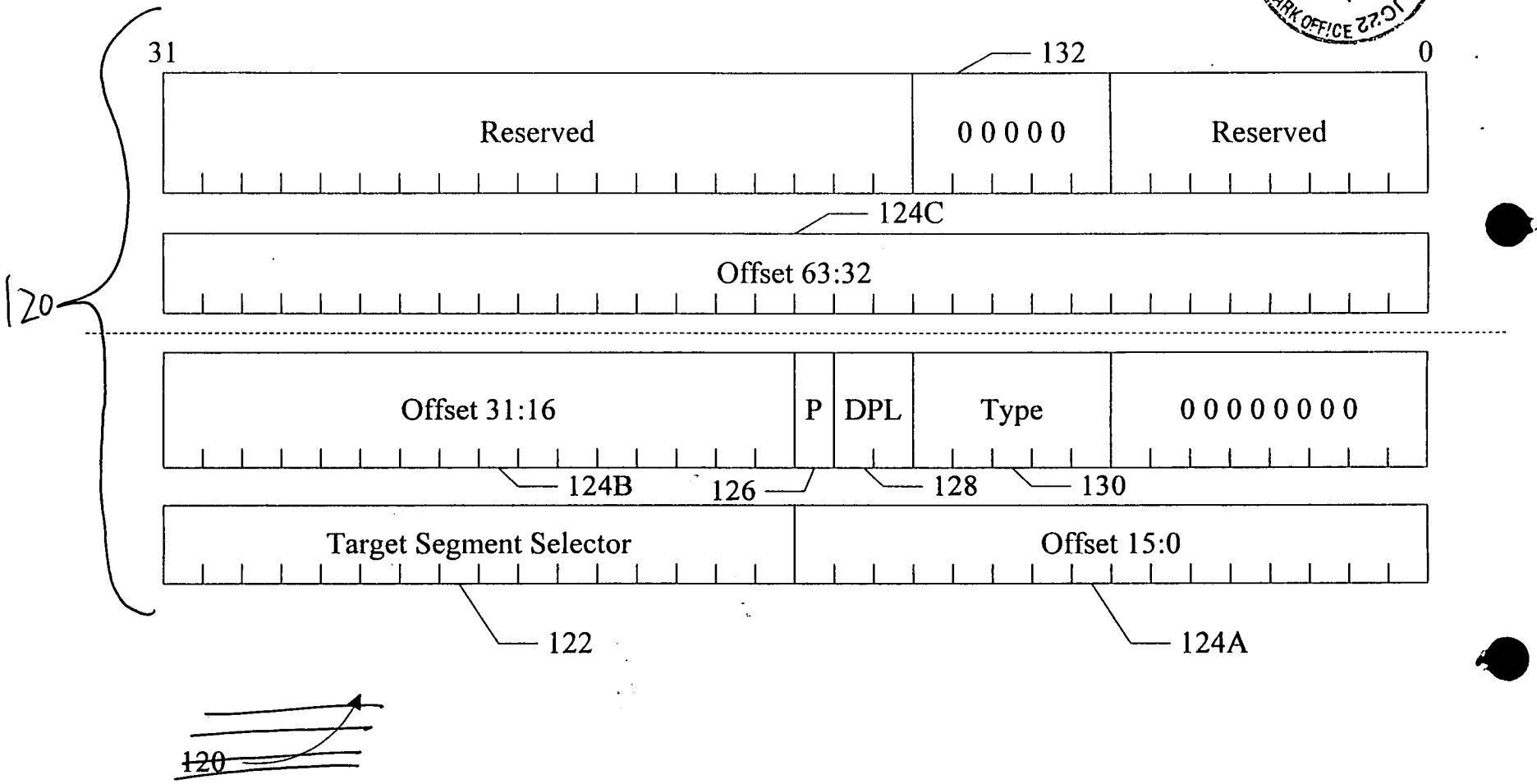

Fig. 9

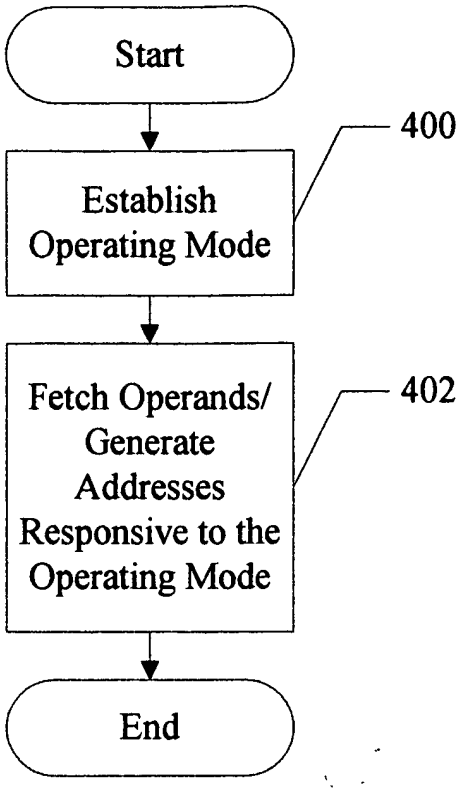

Fig. 13